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DOCKET NO. P05514 (NATI15-05514) **PATENT**
Customer No.: 23990

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	FRANCISCO JAVIER GUERRERO MERCADO
Serial No.	:	10/619,169
Filed	:	July 14, 2003
For	:	LOW POWER COMPARATOR WITH FAST PROPAGATION DELAY
Group	:	2816
Examiner	:	Tuan Thieu Lam

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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APPELLANT'S REPLY BRIEF

This Reply Brief is submitted on behalf of Appellant for the application identified above.

Please charge any additional necessary fees to Deposit Account No. 50-0208.

ARGUMENT

1. The rejection of claims 7–8 and 15–20 under 35 U.S.C. § 112, first paragraph as failing to comply with the enablement requirement.

a. The limitation "wherein the pulsed bias current comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock."

With respect to rejection of claims reciting bias current pulses and output sampling triggered by different system clock edges for lack of enablement, the Examiner's Answer states:

> In this instant, the specification has failed to describe as to how "the pulsed bias current comprises a pulse at one edge of a system clock and an output of the comparator is sampled at another edge of the system clock of claim 7 is made and/or used. Page 13, lines 12-14 of the specification has briefly mentioned that "pulse generator produces a 390 ns wide pulse on every falling edge of the clk signal, and the comparator output is sampled with the clk signal's rising edge". Figure 3 shows a black box labeled as "Pulse Generator" 301. A careful examination of the box 301, it is noted that there is no clock signal being shown. Similarly, the comparator 100 does not show the clock signal. Therefore, it is unclear as to how the pulsed bias current comprises a pulse at one edge of **a system clock** and an output of the comparator is sampled at **another edge of the system clock** is performed without undue experimentation.

Examiner's Answer, page 3 (emphasis in original). The Examiner's rationale thus appears to be that, because a system clock input is not explicitly shown in the drawings for the Pulse Generator 301 and the comparator 100, it would require undue experimentation for those skilled in the art to determine that the system clock should be routed those functional units. The Examiner does not dispute – and indeed implicitly concedes – that system clock signals are known in the art for coordination of various functional units within an integrated circuit:

> Although, global or system clock signal may be used to coordinate various components in a system, it is still unclear as to how the pulsed biased current is generated from the system clock. This pulsed biased current is being used to bias the input gain stage, one of the inventive features of the present invention, thus providing a gain. The specification briefly mentions that pulse current is produced (page 13, lines 12-14). Since the pulsed current bias is a critical feature of the present invention, it is considered an undue experimentation for one skilled in the art to have to determine how to produce a pulse generator that are capable of generating the pulsed current bias as disclosed in the specification.

Examiner's Answer, pages 7-8. In fact, the specification does more than "briefly mention" that the pulse current is produced. Rather, the specification notes that the specific pulse generator circuit is not depicted in Figure 1, but then provides an express description of the pulsed bias current for the exemplary embodiment as being produced on every falling edge of the system clock ("clk") signal, with a specific width or duration relative to the duration of the system clock cycles (390 ns/10 μs), and that the comparator output is sampled on every subsequent rising edge of the system clock signal:

> [0029] *A pulse generator (not shown in FIGURE 1) coupled to the comparator 100 produces the 390 [ns] bias current pulse.* Transistors within comparator 100 are sized for 600 nA of current, and the 2 mV built-in hysteresis and voltage limiting functions are added over existing comparator designs. The analog inputs are expected to reach their steady state before *the falling edge of the system clock (clk) signal*, where the system clock period is 20 μs and the clock duty cycle is 50%. *The pulse generator produces a 390 ns wide pulse* ***on every falling edge of the clk signal, and the comparator output out is sampled with the clk signal's rising edge***.

Specification, page 13, lines 3-14 (emphasis added). The specification thus teaches those skilled in the art that the pulsed bias current is triggered by the falling edge of *every* 20 μs system clock cycle, with a duration (in the exemplary embodiment) of 390 ns (or 3.9% of the 10 μs system clock pulse

for a 20 μs clock with a 50% duty cycle), and the comparator output is sampled at every subsequent rising edge of the system clock clk. Against this description of explicit parameters, the Examiner has not explained why those of ordinary skill would be confused by the absence of express depict of clock inputs to Pulse Generator 301 or comparator 100, or why "undue" experimentation would be required to use known pulse generators to create a pulse generator operating with the described parameters.

In disputing the inconsistency of the art rejections with the assertion of lack of enablement, the Examiner's Answer differentiates the recitation of a simple pulsed bias current from the recitation of a pulses generated in association with the system clock:

> Appellant argues that the application of current Ib of Lim et al. reference and Ic of Heinrich reference to anticipate the "pulse bias current" is contradictory with the rejection of claims 7 and 15 under 35 USC 112, first paragraph is not persuasive. Claims 1-3 and 10-11 (anticipated by Lim); 1-3, 8-11 and 16, 17 (Heinrich) do not call for the pulsed bias current generated in associated with the system clock and the output comparator.

Examiner's Answer, page 8. It should be noted that the drawings do, in fact, depict "pulsed biad current ["ibiaspulse"] generated in associated with . . . the output comparator." At best, the Examiner's complaint can only be that generation of edge-triggered pulses somehow requires "undue" experimentation.

Contrary to the Examiner's position, the production of edge-triggered pulses was and is well known to those of ordinary skill in the art. *Heinrich*, for example,[1] depicts in Figures 2 and 3 that a reference pulse Vref is triggered by the edges of control signal Ic1 pulses:

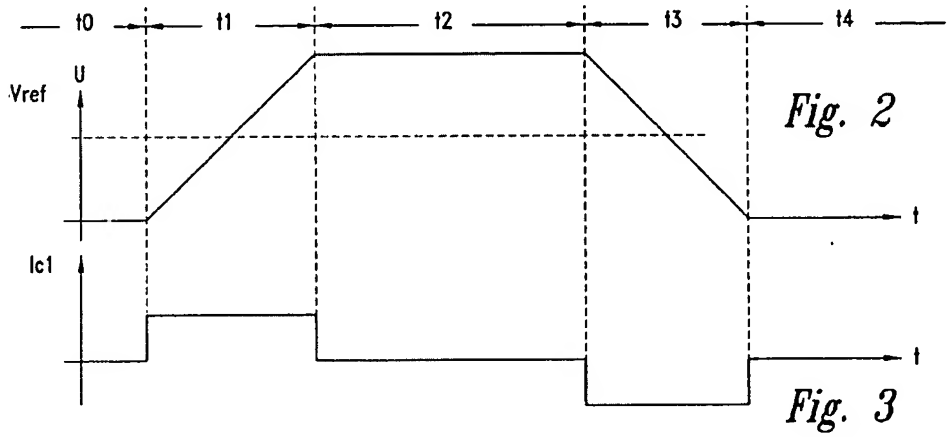

Fig. 2

Fig. 3

The difference between the edge-triggered pulses within the claims and those in *Heinrich* is that the edge-triggered pulses are triggered by every falling edge of the system clock, not by edges of a separate control signal. However, given the admitted knowledge of using a system clock signal to coordinate operation an a circuit, it is unclear how the basis of using the system clock rather than a different control signal could require "undue" experimentation. Does the Examiner suggest that controlling a pulse generator with a cyclic system clock signal requires modification over controlling

[1] Techniques for producing edge-triggered pulses were well-known to those skilled in the art at the time the application was filed. For example, U.S. Patent No. 6,380,779 entitled EDGE-TRIGGERED, SELF-RESETTING PULSE GENERATOR and issued April 30, 2002 discloses such techniques in conjunction with enabling sense amps within a memory. One skilled in the art would recognize that the circuits disclosed therein can readily be applied to triggering a bias current pulse and/or sampling a comparator output. No undue experimentation is required to produce current pulses, edge-triggered or otherwise.

the same pulse generator with a different control signal that may be cycled between various states? Or is routing of the system clock signal the sole source of "undue" experimentation proposed by the Examiner? Accordingly, the Examiner has not identified any specific reason – other than the "criticality" of the feature – why any experimentation required to implement a pulse at one edge of a system clock would be "undue," particularly in light of the specification's description of exemplary parameters for such pulse generation.

b. The limitations "wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a bias current with a defined first level value or in a second mode in which the input gain stage is biased by a bias current with a different second level value," "wherein the comparator selectively operates in a first mode in which the input gain stage is biased by a continuous bias current or in a second mode in which the input gain stage is biased by the pulsed bias current," and "a comparator selectively operating in a first mode in which an input gain stage of the comparator is biased with a pulsed bias current and a second mode in which the input gain stage is biased with a continuous bias current."

With respect to the rejection of claims reciting operation in first and second modes for lack of enablement, the Examiner's Answer states:

> [T]he specification fails to describe as to how the mode of operation is selected. Therefore, it would be undue experimentation for one skilled in the art to try to determine how to make a comparator whose bias current is at different level in different modes of operation.

Examiner's Answer, page 8. However, the claims do not recite **selection** of different modes of operation and/or bias current levels, merely that the comparator be capable of operating in different modes. The question of "how the mode of operation is selected" is irrelevant to whether a

comparator capable of operating in different modes has been enabled. Selection is performed by control functions not pertinent to the subject matter claimed. Such external selection results in different bias currents (constant or pulsed) driving the amplifier (Specification, paragraph [0023]), such that selection within the claimed subject matter is shown. Moreover, the specification provides guidance as to how such selection might be controlled: based on propagation delay versus power consumption. See Specification, paragraphs [0028]-[0029].

Regardless, the cited prior art references teach selection of different modes within comparators operating in different modes, including an operating mode and a power saving mode in *Lim* and selection of different bias current levels in *Heinrich*. *Lim*, column 7, lines 36–37; *Heinrich*, Figure 3.

c. The limitation "a current source producing the pulsed or continuous bias current and controlled by the input signal."

In attempting to support the baseless rejection of claims reciting controlling a current source producing either a pulsed or continuous bias current by an input signal, the Examiner's Answer states:

> Regarding the rejection of claim 19 as being non-enablement, appellant points to figure 1 showing the equivalent circuit of figure 1 and concludes that no undue experiment would be required for those skilled in the art to implement the features of claim 19 is not persuasive. Figure 1 shows parameter gm as a pulse controlling the current source (11) for producing a pulsed or continuous bias current. However, the appellant fails to point out as how to implement a circuit in which the **parameter** gm is generated and a current source is controlled by the **parameter** gm is producing the pulsed or continuous bias current. Therefore, it is unclear as to how current

source biased by pulsed or continuous bias current and controlled the input signal" is achieved without undue experimentation.

Examiner's Answer, page 9 (emphasis in original). As previously noted, Figure 1 depicts a variable current source I1 within the first (input) gain stage 101 producing bias current ibias and controlled by pulsed (or continuous) transconductance signal gm in a manner similar to Figure 4 (Figure 5 as filed):

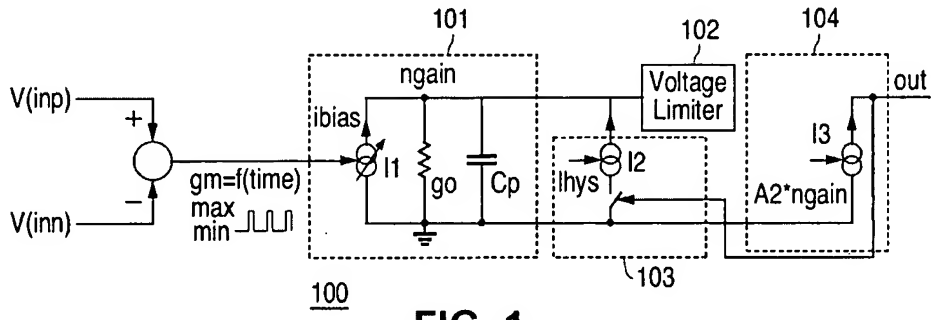

FIG. 1

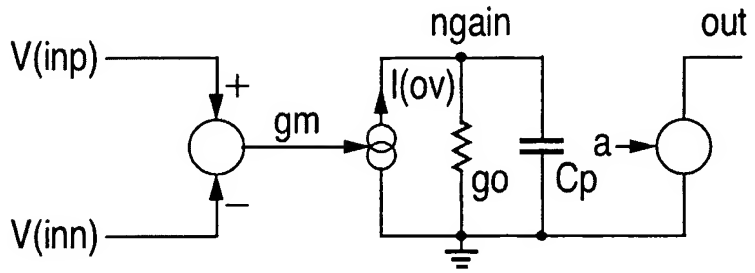

FIG. 5

The specification teaches that the transconductance parameter gm is a function of an input differential pair of CMOS or bipolar junction transistors (now shown in FIGURES 1 or 4):

> [0002] As illustrated in the equivalent circuit diagram depicted in FIGURE 5, integrated circuit comparators typically include: a bias system generating a defined current bias to each transistor; an input differential pair--either complementary metal oxide semiconductor (CMOS) or bipolar junction transistors--that, for a given overdrive voltage V(ov)=(V(inp)-V(inn)) generate a differential current given by I(ov)=gm*V(ov), where gm is the transconductance of the input differential pair at the steady-state operating point V(ov)=0 volts (V); a gain stage node ngain converting the current I(ov) to (in the CMOS case) a voltage gain and having a transition speed depending on the overdrive current I(ov) available, the voltage excursion required between the high and low levels at the ngain node, and the capacitive load at the ngain node, including any Miller capacitance from the comparator's output stage; and a gain stage assuring a given slew rate at the comparator output out.

Specification, ¶ [0002]. Those skilled in the art will understand that when the input transistors are continuously switched on, the transconductance parameter gm will have a continuous value while applying a pulsed control signal to the gates of the input transistors will produce a pulsed transconductance parameter gm.

In addition, the Examiner's Answer cites *Sedra et al* as teaching that the transconductance parameter gm may be produced across the collector and emitter of a bipolar transistor:

> Sedra et al. clearly proves that transconductance parameter is directly proportional to the collect current of a bipolar transistor. Thus, the collector current along the collect-emitter path of the input transistors Q8 and Q9 is the input signal (gm).

Examiner's Answer, pages 9–10. Once again, the Examiner's Answer makes an unsupportable assertion – that undue experimentation would be required for those skilled in the art to "to implement a circuit in which the parameter gm is generated" – contrary to the asserted prior art rejections.

2. The rejection of claims 1–3 and 10–11 under 35 U.S.C. § 102(e) as being anticipated by *Lim*.

The Examiner's Answer asserts that, contrary to the specification, the term "pulsed" and the the claim limitation "pulsed bias current" does not require pulsing of the bias current in accordance with the system clock, but is instead satisfied by the continuous bias current of *Lim*, which may selectively be turned on and off. However, the final rejection and the Examiner's Answer offer absolutely no evidentiary support for such an interpretation of the term "pulsed." No use of the term "pulsed" in *Lim* to describe the continuous bias current of Figure 5c (as opposed to the trigger signal and the output signal of the comparator disclosed in *Lim*) has ever been identified, and no dictionary or technical definition has been cited supporting such an interpretation.

Moreover, the proffered interpretation is inconsistent with the use of the term within the specification. The exemplary embodiments disclosed within the specification all define the "pulse bias current" as having a duration shorter than the system clock cycle. Specification, paragraph [0029] (390 ns versus 20 μs). Moreover, the specification teaches that the pulsed bias current pulses are triggered at every falling edge of the system clock clk, which unequivocally ***requires*** the pulsed bias current to consist of pulses having a duration defined by the system clock cycle. Accordingly, the suggested interpretation of the term "pulsed" and the claim limitation "pulsed bias current" are completely arbitrary and capricious.

3. The rejection of claims 1–3, 8–11 and 16–17 under 35 U.S.C. § 102(e) as being anticipated by *Heinrich*.

The Examiner's Answer asserts that, contrary to the specification, the term "pulsed" and the the claim limitation "pulsed bias current" does not require pulsing of the bias current in accordance with the system clock, but is instead satisfied by the varying-level but continuous bias current of *Heinrich* between the higher level and the lower level. However, the final rejection and the Examiner's Answer offer absolutely no evidentiary support for such an interpretation of the term "pulsed." The term "pulsed" does not appear anywhere within *Heinrich*, and in particular is not employed to describe the varying continuous bias current Ic1 of Figure 3. No dictionary or technical definition has been cited supporting the interpretation suggested in the final rejection and Examiner's Answer. Accordingly, the suggested interpretation of the term "pulsed" and the claim limitation "pulsed bias current" are completely arbitrary and capricious.

CONCLUSION

The subject matter of claims 7–8 and 15–20 is enabled by the specification as filed. Therefore, the rejection of claims 7–8 and 15–20 under 35 U.S.C. § 112, first paragraph is improper. The cited references fail to disclose every limitation of the claimed invention. Therefore, the rejections of claims 1–3, 8–11 and 16–17 under 35 U.S.C. § 102 are improper. Applicant respectfully requests that the Board of Appeals reverse the decision of the Examiner below rejecting pending claims 1–3, 7–11 and 15–20 in this application.

Respectfully submitted,

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Date: Sept. 21, 2007

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